

### REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on July 13, 2001, and the references cited therewith.

Claims 20, 25, 30, 31, 38, 41, 44, 45, 49, 51, 53 and 55 are amended; as a result, claims 20-56 are now pending in this application.

#### Double Patenting Rejection

Claims 20-26, 27-56 were rejected under the judicially created (i.e., non-statutory) doctrine of double patenting over claims 1-7 of U.S. Patent No. 6,156,604, or claims 1-22 of U.S. Patent No. 6,156,607.

A Terminal Disclaimer in compliance with 37 CFR 1.321(b)(iv) is enclosed herewith to overcome these rejections.

#### §102 Rejection of the Claims

Claims 20, 21, 23-25, 27-28, 30, 32, 34, 35, 37, 39, 41, 42, 44, 46, 48-53 were rejected under 35 USC § 102(b) as being anticipated by Gotou (U.S. 5,001,526).

Gotou teaches forming a DRAM cell using so-called "bonded wafer" technology, as describe in col. 4, line 41 through col. 5, line 9; FIGS. 4A, 4B and 5. This technology involves forming layers on *two separate substrates*, interfacing the substrates, bonding them together and then polishing one of the substrates to obtain a multi-layered structure (FIG. 6).

Applicant's invention does not employ bonded wafer technology. Rather, Applicant's invention is formed with and upon a *single substrate*.

Accordingly, Applicant has amended independent claims 20, 41, 49, 51, 53 and 55 to distinguish their invention from the wafer bonding process of Gotou by including the limitation that the device be formed from a *single substrate*. Likewise, independent claim 25 has been amended to include the limitation that the layers be epitaxially grown atop one another (claim 25) to distinguish from the wafer bonding process taught by Gotou.

Applicant respectfully submits that the above-described amendments render the aforementioned claims, as well as the claims depending therefrom, patentable. Applicant thus

**PRELIMINARY AMENDMENT**

Serial Number: 09/551,027

Filing Date: April 17, 2000

Title: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

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Dkt: 303.379US2

respectfully requests reconsideration and withdrawal of the rejection of the above-cited claims under 35 USC § 102(b) based on Gotou.

*§103 Rejection of the Claims*

Claims 22, 29, 31, 32, 35, 38, 40, 43, 45, 47, 54-56 were rejected under 35 USC § 103(a) as being unpatentable over Gotou (U.S.5,001,526) taken with Kimura et al. (5,177,576). Applicant submits that the amendments made to the above-identified claims to overcome the rejection under 35 USC § 102(b) based on Gotou also serve to overcome the rejection under 35 USC § 103(a) based on Gotou. Applicant thus respectfully requests reconsideration and withdrawal of the rejection under 35 USC § 103(a) of the above-cited claims based on Gotou and Kimura.

*Conclusion*

Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration and withdrawal of the rejections, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612- 373-6913) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

WENDELL P. NOBLE ET AL.

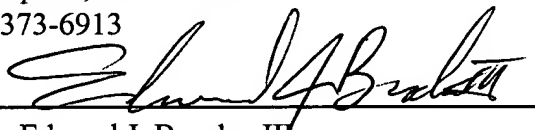
By their Representatives,

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Date

9/19/2001

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This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box CPA, Washington, D.C. 20231.